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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,060	02/26/2002	Kyle Spring	IR-1821 (2-2833)	4378

2352 7590 11/29/2002

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[REDACTED] EXAMINER

RAO, SHRINIVAS H

[REDACTED] ART UNIT

[REDACTED] PAPER NUMBER

2814

DATE MAILED: 11/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/083,060	SPRING ET AL. <i>[Signature]</i>
	<b>Examiner</b>	<b>Art Unit</b>
	Steven H. Rao	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 16 September 2002.

2a) This action is **FINAL**.                  2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-3 is/are pending in the application.

4a) Of the above claim(s) 3 is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1 and 2 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
 If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

#### Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input checked="" type="checkbox"/> Interview Summary (PTO-413) Paper No(s). <u>4</u> .
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.	6) <input type="checkbox"/> Other: _____

***Response to Amendment***

Applicants' amendment filed on September 16, 2002 has been entered on September 24, 2002.

Therefore claims 1-2 as originally filed are currently pending in the application.

***Election/Restrictions***

This application contains claim 3 drawn to an invention nonelected claims with out traverse in Paper No. 3 A . A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

***Drawings***

The corrected or substitute drawings were received on September 16, 2002. These drawings have been placed in the file and upon approval thereof by the drafts person will be entered.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Hshieh et al. (U.S. Patent No. 5,729,037 herein after Hshieh) for reasons previously stated and reproduced below.

With respect to claim1, Hshieh describes a vertical MOSFET including : a substrate of first conductivity type ( Fig. 2 A # 105, P-substrate, col. 3 line 65), a channel region of second conductivity type diffused into the substrate ( region between source and drain in fig. 3), a gate disposed at least partially over the channel region ( fig. 3 #125 not identified, col. 4 line 52), a source region of a first conductivity type disposed proximate to the gate and adjacent to the channel region ( fig. 3 # 150), col. 4 line 57), the channel region includes a depletion implant area proximate to the gate, the depletion implant species being of the second conductivity type to reduce the concentration of the first conductivity type in the channel region without decreasing the conductivity in the drain region. ( Col. 4 lines 54-67).

With respect to claim 2, Hshieh describes a vertical MOSFET including : wherein the substrate includes a substrate of first conductivity type ( Fig. 2 A # 105, P-substrate, col. 3 line 65), and a second region of the first conductivity type disposed on the first region and having a concentration of carriers which is less than the concentration of carriers in the first region. ( Fig. @ c # 135 and 150 of p + type, it is tht due to the position of the layers in the substrate that the first region has more concentration than the second layer) further as only the second region is subject to special body-dopant it is inherent that only the second region has less concentration of carriers ( because some of the carriers present prior to the dopant step are replaced by the dopants), than the concentration of carriers in the first region.

### Response to Arguments

Applicant's arguments filed 9/24/02 have been fully considered but they are not persuasive for the following reasons.

Applicants' contention that the structure shown by Hshieh does not include an implant area in which the implant species of the second conductivity type reduce the concentration of the first conductivity type is not persuasive because Hshieh in fig. 4b and col. 5 lines 51-67 describes an area wherein the concentration of the dopants is changed by the implantation of dopant of second conductivity type .

A method for fabricating a MOSFET transistor on a substrate 105 is also disclosed in this invention. The method includes the steps of (a) forming an epi-layer 110 of a first conductivity type as a drain region on the substrate and forming an initial oxide layer 115 and then forming a gate oxide layer 120 thereon followed by depositing an overlaying polysilicon layer 125; (b) applying a poly mask for etching the polysilicon layer to define a plurality of poly gates 125; (c) carrying out a body implant of a second conductivity type followed by performing a body diffusion for forming a plurality of body regions 135; (d) applying a source blocking mask for implanting a plurality of source regions 150 in the body regions with the first conductivity type followed by removing the source blocking mask 145; (e) forming a source-dopant segregation reduction layer including a LPCVD nitride layer 154 on top of the MOSFET

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

It is noted that as the same reference as previously applied is also applied here , this forms a separate basis for making this action Final.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

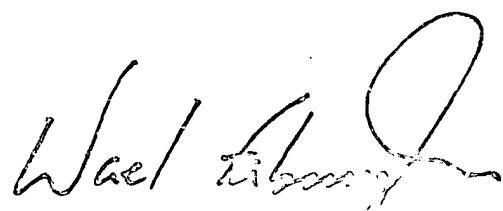
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7463926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

SR  
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November 25, 2002



SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER (200)